

REMARKS

Applicants respectfully request favorable reconsideration of this application.

The outstanding Office Action acknowledged the cancellation of Claims 2-10 in the Preliminary Amendment dated July 11, 2003, and further rejected Claim 1 for same invention double patenting over Claim 1 of prior U.S. Patent 6,608,784. However, Claim 1 was cancelled in favor of new Claim 11 by Supplemental Preliminary Amendment dated November 24, 2003. Copies of the Supplemental Preliminary Amendment and the postcard receipt are attached for the Examiner's convenience. It is apparent that the outstanding double-patenting rejection is inapplicable to Claim 11.

Accordingly, Applicants respectfully request that the outstanding rejection be withdrawn and that a favorable action be given with respect to Claim 11.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§1.16 and 1.17 which may be required by this paper, and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, then such extension is hereby requested.

MWS:jab

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September 1, 2004

Respectfully submitted,

By: 

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XA-9624A
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Motoki KANAMORI et al.

Appln. No: 10/616,955

Group Art Unit: 2818

Filed: July 11, 2003

For: NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE

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SUPPLEMENTAL PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to examination, please amend the above-identified patent application as indicated below.

Amendments to the claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 3 of this paper.

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

Claims 1-10 (Cancelled)

11. (New) A non-volatile memory comprising an error correction circuit and a storage device,

wherein inputted data is written to said storage device corresponding to a first address, the written data is read from said storage device when a write error has occurred, said error correction circuit judges whether the read data can be corrected, a write operation ends if the read data can be corrected, said inputted data is written to said storage device corresponding to a second address which differs from said first address if the read data cannot be corrected.

REMARKS

Claim 1 has been cancelled without prejudice or disclaimer.

New Claim 11 is presented for examination at this time.

An action on the merits of Claim 11 is respectfully solicited.

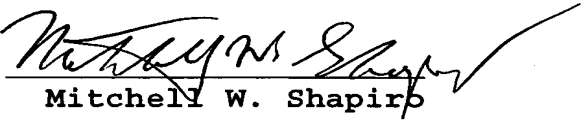
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November 24, 2003.



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Applicant: Motoki KANAMORI et al.

XA-9624A

Appln. No.: 10/616,955

T3351-907770A

Filed: July 11, 2003

For: NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE

Attached: Supplemental Preliminary Amendment;
Request for Refund



RECEIVED IN U.S. PATENT AND TRADEMARK OFFICE: